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EXAMINER
HSU, JONI

ART UNIT	PAPER NUMBER
2676	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/604,524	LEE, HIN-KWAI	
	Examiner	Art Unit	
	Joni Hsu	2676	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6, 8-16, 19, 20* is/are rejected.

7)☒ Claim(s) *7,17 and 18* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *7/28/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification

1. The disclosure is objected to because of the following informalities: According to MPEP § 608.01 (m), the present Office practice is to insist that each claim must be the object of a sentence starting with "I (or we) claim," "The invention claimed is" (or the equivalent). The phrase "Claims" is not considered equivalent to these appropriate phrases. Appropriate correction is required.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1 and 3 are rejected under 35 U.S.C. 102(b) as being anticipated by Schlapp (US005579473A).

4. With regard to Claim 1, Schlapp describes a graphics system comprising a dynamic-random-access memory (DRAM) for storing graphics data (Col. 4, lines 41-51); a static random-access memory (SRAM) (56, Figure 2) for storing pixels in a frame buffer (Col. 4, lines 59-61);

a first bus to the SRAM (112); a second bus to the DRAM (110); a refresh controller (83, Figure 1; Col. 2, lines 8-12), coupled to the SRAM through the first bus, and coupled to the DRAM through the second bus (Col. 4, lines 27-35), for reading pixels from the frame buffer for display to a display device; a graphics engine (70), coupled to the SRAM through the first bus, and coupled to the DRAM through the second bus, for reading and writing graphics data (Col. 3, line 60-Col. 4, line 19); and a dual-layer arbiter (330, Figure 3), receiving requests from the refresh controller to access the SRAM and requests from the graphics engine to access the DRAM, and also receiving requests from the refresh controller to access the DRAM and requests from the graphics engine to access the SRAM (Col. 13, line 55-Col. 14, line 9), the dual-layer arbiter allowing simultaneous access of the DRAM and SRAM (Col. 17, lines 20-26) when the refresh controller requests access of the SRAM (Col. 2, lines 8-12; Col. 4, lines 27-35) and the graphics engine requests access of the DRAM (Col. 3, line 60-Col. 4, line 19), but the dual-layer arbiter delaying access of the DRAM by the graphics engine when the refresh controller access the DRAM, whereby the dual-layer arbiter allows simultaneous DRAM and SRAM access or arbitrated access of either the DRAM or the SRAM (Col. 17, lines 39-53).

5. With regard to Claim 3, Schlapp describes that the SRAM has a higher speed than the DRAM (Col. 4, lines 59-61), and therefore has a smaller access time.

6. Thus, it reasonably appears that Schlapp describes or discloses every element of Claims 1 and 3 and therefore anticipates the claims subject.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

9. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Schlapp (US005579473A) in view of Yamashita (US006313844B1).

Schlapp describes a SRAM (56, Figure 2; Col. 3, lines 26-29), and the SRAM inherently stores data as states of a bi-stable circuit. This is inherent because all SRAM devices store data as states of a bi-stable circuit, according to the definition found on the free-definition website.

However, Schlapp does not teach that the DRAM stores data as charges on capacitors that periodically require refreshing of the charges. However, Yamashita describes a graphics system comprising a DRAM (16, Figure 9; Col. 14, lines 18-21), a SRAM (17; Col. 15, lines 8-19), a refresh controller (30; Col. 16, lines 41-45), and a graphics engine (12; Col. 15, lines 24-

31). Yamashita describes that the DRAM stores data as charges on capacitors that periodically require refreshing of the charges (Col. 1, lines 37-43).

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to modify the device of Schlapp so that the DRAM stores data as charges on capacitors that periodically require refreshing of the charges as suggested by Yamashita because Yamashita suggests that all DRAM devices store data in this manner (Col. 1, lines 37-43). This is well-known in the art.

10. Claims 4-6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Schlapp (US005579473A) in view of Rodgers (US006131140A).

11. With regard to Claim 4, Schlapp is relied upon for the teachings as discussed above relative to Claim 3. Schlapp describes that the first bus (112, Figure 1) is coupled to the refresh controller (83; Col. 2, lines 8-12; Col. 4, lines 27-35) and the graphics engine (70; Col. 3, line 60-Col. 4, line 19) and the second bus (110) is coupled to the refresh controller (Col. 4, lines 27-35) and the graphics engine (Col. 3, line 60-Col. 4, line 19). Schlapp describes a dual-layer arbiter (330, Figure 3), receiving requests from the refresh controller to access the SRAM and requests to access the DRAM, and also receiving requests from the graphics engine to access the DRAM and requests to access the SRAM (Col. 13, line 55-Col. 14, line 9).

However, Schlapp does not teach a first mux and a second mux for connecting the SRAM and the DRAM to the refresh controller and the graphics engine. However, Rodgers describes a first mux (201a, Figure 3a) connecting the SRAM (105a) to other components (Col. 6, line 66-

Col. 7, line 4) and a second mux (208) connecting the DRAM (109, Figure 2) to other components (Col. 8, lines 39-46).

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to modify the device of Schlapp to include a first mux and a second mux for connecting the SRAM and the DRAM to the refresh controller and the graphics engine as suggested by Rodgers. A multiplexer is a device for taking several separate digital data streams and combining them together into one data stream of a higher data rate. Multiplexers have the advantage of allowing multiple data streams to be carried from one place to another over one physical link, which saves cost. Multiplexers are well-known in the art, widely used, and can be found in many publications, such as the *Wikipedia Encyclopedia*.

12. With regard to Claim 5, Schlapp describes that the first bus can transfer data to the SRAM at a same time that the second bus transfers data to the DRAM, as discussed in the rejection for Claim 1.

However, Schlapp does not teach a first mux and a second mux. However, Rodgers describes a first mux and a second mux, as discussed in the rejection for Claim 4.

13. With regard to Claim 6, Schlapp describes that the first bus (112, Figure 1) comprises address, data, and control signals for controlling access to the SRAM (56, Figure 2; Col. 3, lines 26-29); wherein the second bus (110, Figure 1) comprises address, data, and control signals for controlling access to the DRAM (Col. 3, lines 21-25) (Col. 4, lines 27-35).

14. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Schlapp (US005579473A) in view of Rodgers (US006131140A), further in view of Laksono (US006288729B1).

Schlapp and Rodgers are relied upon for the teachings as discussed above relative to Claim 4. Schlapp describes that the dual-layer arbiter allows simultaneous access of the DRAM and SRAM when the refresh controller requests access of the SRAM and the second graphics engine requests access of the DRAM, but the dual-layer arbiter delaying access of the DRAM by the second graphics engine when the refresh controller access the DRAM, as discussed in the rejection for Claim 1. Rodgers describes a first mux (201a, Figure 3a) connecting the SRAM (105a) to other components (Col. 6, line 66-Col. 7, line 4) and a second mux (208) connecting the DRAM (109, Figure 2) to other components (Col. 8, lines 39-46), as discussed in the rejection for Claim 4.

However, Schlapp and Rodgers do not teach a second graphics engine. However, Laksono describes a second graphics engine (Col. 5, lines 57-62) coupled to the system memory (16, Figure 1) through the first bus (22), and coupled to the graphics memory (20) through the second bus, for reading and writing graphics data; wherein the dual-layer arbiter (26) further receives requests from the second graphics engine to access the graphics memory, and requests from the second graphics engine to access the system memory (Col. 4, lines 35-38), and the dual-layer arbiter is connected to the second graphics engine, the system memory, and the graphics memory. It is well-known in the art that the system memory is usually SRAM and the graphics memory is usually DRAM, so the system memory is considered to be SRAM and the graphics memory is considered to be DRAM.

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to modify the devices of Schlapp and Rodgers to include a second graphics engine as suggested by Laksono because Laksono suggests the advantage of multiple graphics engines being able to share the same memory, making more use out of the memory (Col. 2, lines 4-9).

15. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Schlapp (US005579473A), in view of Rodgers (US006131140A), further in view of Laksono (US006288729B1), further in view of Lavelle (US006812929B2).

Schlapp, Rodgers, and Laksono are relied upon for the teachings as discussed above relative to Claim 8.

However, Schlapp, Rodgers, and Laksono do not teach that the graphics engine is a video overlay engine or a 3-dimensional graphics engine. However, Lavelle is similar to Schlapp and has a DRAM (914, Figure 8) for storing graphics data and a SRAM (930) for storing pixels in a frame buffer (Col. 10, lines 47-49). Lavelle also describes that the graphics engine is a video overlay engine (190, Figure 6; Col. 9, lines 33-38).

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to modify the devices of Schlapp, Rodgers, and Laksono so that the graphics engine is a video overlay engine as suggested by Lavelle. A video overlay engine is needed in order to place a full-motion video window on the display screen. Video overlay engines are well-known in the art, widely used, and found in many publications, such as the *Webopedia Computer Dictionary*.

16. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Schlapp (US005579473A) in view of Lavelle (US006812929B2), further in view of Rodgers (US006131140A).

Schlapp describes a dual-layer arbitrated graphics system comprising a dynamic-random-access memory (DRAM) for storing graphics data (Col. 3, lines 21-25); a static random-access memory (SRAM) (56, Figure 2) for storing display pixels in a frame buffer (Col. 3, lines 26-29); an SRAM bus (112, Figure 1) for transferring data to and from the SRAM; a DRAM bus (110) for transferring data to and from the DRAM (Col. 4, lines 27-35); a refresh controller (83) coupled to drive display pixels to a display (Col. 2, lines 8-12). Schlapp describes that the first bus (112, Figure 1) is coupled to the refresh controller (83; Col. 2, lines 8-12; Col. 4, lines 27-35) and the graphics engine (70; Col. 3, line 60-Col. 4, line 19) and the second bus (110) is coupled to the refresh controller (Col. 4, lines 27-35) and the graphics engine (Col. 3, line 60-Col. 4, line 19). Schlapp describes a dual-layer arbiter (330, Figure 3), receiving requests from the refresh controller to access the SRAM and requests to access the DRAM, and also receiving requests from the graphics engine to access the DRAM and requests to access the SRAM (Col. 13, line 55-Col. 14, line 9). Schlapp describes a dual-layer arbiter (330, Figure 3) is coupled to receive requests from the refresh controller (83, Figure 1; Col. 2, lines 8-12) and requests from the graphics engine (102), for arbitrating access to the SRAM (56, Figure 2; Col. 4, lines 59-61) when both the refresh controller and the graphics engine request access to the SRAM, and for arbitrating access to the DRAM (Col. 3, line 60-Col. 4, line 19), but allowing simultaneous or parallel access to both the SRAM and to the DRAM when the refresh controller and the graphics engine request access to different memories; wherein the dual-layer arbiter generates the first

select signal to the SRAM and the second select signal to the DRAM in response to the dual-layer arbiter arbitrating access or allowing parallel access (Col. 17, lines 20-26), whereby parallel access to the SRAM and to the DRAM is allowed when arbitrating access is not required by requests (Col. 17, lines 39-53),

However, Schlapp does not teach that the graphics engine is a first overlay engine. However, Lavelle describes a DRAM (914, Figure 8) for storing graphics data, a SRAM (930) for storing display pixels in a frame buffer (Col. 10, lines 47-49) as discussed in the rejection for Claims 1 and 9, and a first overlay engine (190, Figure 6) that manipulates graphics data (Col. 9, lines 33-38), as discussed in the rejection for Claim 9.

However, Schlapp and Lavelle do not teach a first mux and a second mux for connecting the SRAM and the DRAM to the refresh controller and the first overlay engine. However, Rodgers describes a first mux (201a, Figure 3a) connecting the SRAM (105a) to other components (Col. 6, line 66-Col. 7, line 4) and a second mux (208) connecting the DRAM (109, Figure 2) to other components (Col. 8, lines 39-46), as discussed in the rejection for Claim 4.

17. Claims 11 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Schlapp (US005579473A) in view of Lavelle (US006812929B2), further in view of Rodgers (US006131140A), further in view of Kotzur (US006389480B1).

18. With regard to Claim 11, Schlapp, Lavelle, and Rodgers are relied upon for the teachings as discussed above relative to Claim 10.

However, Schlapp, Lavelle, and Rodgers do not teach that the dual-layer arbiter arbitrates access using round-robin arbitration wherein the refresh controller and the first overlay engine are given equal priority for accessing the SRAM or the DRAM, or using priority arbitration wherein the refresh controller is given higher priority that the first overlay engine for accessing the SRAM or the DRAM. However, Kotzur describes a dual-layer arbiter (504, Figure 5A; Col. 18, lines 53-55) that arbitrates access using round-robin arbitration (Col. 2, line 58-Col. 3, line 29; Col. 19, lines 3-5; Col. 28, line 64-Col. 29, line 25) wherein the refresh controller (210, Figure 4) and other ports are given equal priority for accessing the SRAM (650, Figure 6) or the DRAM (638).

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to modify the devices of Schlapp, Lavelle, and Rodgers so that the dual-layer arbiter arbitrates access using round-robin arbitration wherein the refresh controller and the first overlay engine are given equal priority for accessing the SRAM or the DRAM, or using priority arbitration wherein the refresh controller is given higher priority that the first overlay engine for accessing the SRAM or the DRAM as suggested by Kotzur because Kotzur suggests the advantage of providing an efficient system for determining priority for selecting and for servicing multiple ports (Col. 2, lines 38-40). Round-robin arbitration is well-known in the art and widely used.

19. With regard to Claim 12, Schlapp describes a refresh controller request signal, generated by the refresh controller (83, Figure 1; Col. 2, lines 8-12) and sent to the dual-layer arbiter (330, Figure 3; Col. 13, line 55-Col. 14, line 9), for requesting access to the SRAM (56, Figure 2; Col.

3, lines 26-29) or to the DRAM (Col. 3, lines 21-25) by the refresh controller (Col. 4, lines 27-35). Since the refresh controller accesses both the DRAM and the SRAM, the refresh controller must inherently generate a refresh controller type signal for indicating when access to the SRAM is requested or when access to the DRAM is requested. Schlapp describes a first graphics engine request signal, generated by the first graphics engine (70, Figure 1) and sent to the dual-layer arbiter for requesting access to the SRAM or to the DRAM by the first graphics engine (Col. 3, line 60-Col. 4, line 19). Since the first graphics engine accesses both the DRAM and the SRAM, the first graphics engine must inherently generate a first graphics engine type signal and send it to the dual-layer arbiter, for indicating when access to the SRAM is requested or when access to the DRAM is requested.

However, Schlapp does not teach that the first graphics engine is an overlay engine. However, Lavelle describes that the first graphics engine is an overlay engine, as discussed in the rejection for Claim 9.

20. Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Schlapp (US005579473A) in view of Lavelle (US006812929B2), further in view of Rodgers (US006131140A), further in view of Kotzur (US006389480B1), further in view of Kato (US006070205A).

Schlapp, Lavelle, Rodgers, and Kotzur are relied upon for the teachings as discussed above relative to Claim 12. Schlapp describes a refresh controller (83, Figure 1; Col. 2, lines 8-12) that accesses the DRAM and the SRAM (56, Figure 2) (Col. 4, lines 27-25).

However, Schlapp, Lavelle, Rodgers, and Kotzur do not teach grant signals. However, Kato describes a DRAM refresh controller (1315, Figure 8) and a DRAM (1305) connected to the first bus (1317) (Col. 9, lines 2-5) and a data retention circuit or refresh controller for SRAM and a SRAM (132) connected to the second bus (1319) (Col. 9, lines 28-34), and a graphics engine (1302) that is connected to both the first and second buses (Col. 8, line 64-Col. 9, line 2). Kato describes first and second bus grant signals generated by the dual-layer arbiter (1306, 1307; Col. 7, lines 23-24; Col. 9, lines 21-26). Therefore, a refresh controller grant signal must inherently be generated by the dual-layer arbiter and sent to the refresh controller, to indicate that the refresh controller may access a requested memory; a first graphics engine grant signal, generated by the dual-layer arbiter and sent to the first graphics engine, to indicate that the first graphics engine may access a requested memory.

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to modify the devices of Schlapp, Lavelle, Rodgers, and Kotzur to include grant signals as suggested by Kato because Kato suggests that grant signals are needed so that a refresh controller or a first overlay engine knows when they may access a requested memory (Col. 7, lines 23-24; Col. 9, lines 2-26). Grant signals are well-known in the art and widely used.

21. Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Schlapp (US005579473A) in view of Lavelle (US006812929B2), further in view of Rodgers (US006131140A), further in view of Kotzur (US006389480B1), further in view of Laksono (US006288729B1).

Schlapp, Lavelle, Rodgers, and Kotzur are relied upon for the teachings as discussed above relative to Claim 11. Lavelle describes that the graphics engine is an overlay engine for manipulating the graphics data, as discussed in the rejection for Claim 9. Rodgers describes a first mux and a second mux, as discussed in the rejection for Claim 4. Schlapp describes a dual-layer arbiter that grants access of a graphics engine to the SRAM and a second select signal further indicates when the graphics engine is granted access to the DRAM by the dual-layer arbiter, as discussed in the rejection for Claim 10.

However, Schlapp, Lavelle, Rodgers, and Kotzur do not teach a second graphics engine. However, Laksono describes a second graphics engine, as discussed in the rejection for Claim 8.

22. Claims 15 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Schlapp (US005579473A) in view of Laksono (US006288729B1), further in view of Lavelle (US006812929B2), further in view of Kotzur (US006389480B1).

23. With regard to Claim 15, Schlapp describes a dual-memory arbitrated graphics sub-system comprising dynamic-random-access memory (DRAM) means for storing graphics data (Col. 3, lines 21-25); static random-access memory (SRAM) means (56, Figure 2) for storing display pixels in a frame buffer (Col. 3, lines 26-29); refresh controller means (83, Figure 1) for reading the display pixels from the frame buffer and writing the display pixels to a display during a screen refresh (Col. 2, lines 8-12); a graphics engine means (70) for processing the graphics data to generate display pixels or intermediate graphics data (Col. 3, line 60-Col. 4, line 19); first bus means (112, Figure 1) for transferring address and data to the SRAM means; second bus

means (110) for transferring address and data to the DRAM means (Col. 4, lines 27-35); arbiter means (330, Figure 3; Col. 13, line 55-Col. 14, line 9) allowing simultaneous access of the SRAM means and the DRAM means (Col. 17, lines 20-26).

However, Schlapp does not teach a first and second overlay engine. However, Laksono describes a first graphics engine means for processing the graphics data to generate display pixels or intermediate graphics data; second graphics engine means for processing the graphics data to generate display pixels or intermediate graphics data, as discussed in the rejection for Claim 8.

However, Schlapp and Laksono do not teach that the graphics engines are overlay engines. However, Lavelle describes that the graphics engine is an overlay engine, as discussed in the rejection for Claim 9.

However, Schlapp, Laksono, and Lavelle do not teach the arbiter means as discussed in Claim 15. However, Kotzur describes an arbiter means (504, Figure 5A) with round-robin arbitration for arbitrating access of the SRAM means (506) and the DRAM means (506) from the refresh controller means (210, Figure 4) or other ports, as discussed in the rejection for Claim 11. Therefore, Kotzur inherently describes receiving first requests for access of the SRAM means from the refresh controller means or other ports, and receiving second requests for access of the DRAM means for the refresh controller means or the other ports, for arbitrating among the first requests when received at a same time period to generate a first grant to a first winning requestor, and for arbitrating among the second requests when received at a same time period to generate a second grant to a second winning requestor, first selector means, for selecting the refresh controller means or the other ports for connection to the SRAM means in response to an

indication of the first winning requestor from the arbiter means; and second selector means, coupled to the second bus means, for selecting the refresh controller means or the other ports for connection to the DRAM in response to an indication of the second winning requestor from the arbiter means, whereby three requestors are arbitrated for access of two memories.

24. With regard to Claim 19, Laksono describes a first and second graphics engine means, as discussed in the rejection for Claim 8. Lavelle describes that the graphics engine means is an overlay engine means, as discussed in the rejection for Claim 9. Kotzur describes a refresh controller and other ports, and a round-robin arbitration for selecting the ports, as discussed in the rejection for Claim 11. By definition, a round-robin arbitration has a first round-robin means for alternately selecting as a first winning requestor the refresh controller means or the other ports; and second round-robin means for alternately selecting as the second winning requestor the refresh controller means or the other ports.

25. Claim 16 is rejected under 35 U.S.C. 103(a) as being unpatentable over Schlapp (US005579473A) in view of Laksono (US006288729B1), further in view of Lavelle (US006812929B2), further in view of Kotzur (US006389480B1), further in view of Kato (US006070205A).

Schlapp, Laksono, Lavelle, and Kotzur are relied upon for the teachings as discussed above relative to Claim 15. Schlapp describes that a first bus means (112, Figure 1) is further for transferring control signals to the SRAM means (56, Figure 2; Col. 3, lines 26-29) (Col. 4, lines 27-35); wherein the second bus means (110, Figure 1) is further for transferring control signals to

the DRAM means (Col. 3, lines 21-25; Col. 4, lines 27-35); wherein the first bus means and the second bus means differ in control signals.

However, Yamashita, Laksono, Lavelle, and Schlapp do not teach that the first bus means and the second bus means differ in width of address. However, Kato describes that the first bus means and the second bus means differ in width of address (Col. 10, lines 54-62).

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to modify the devices of Schlapp, Laksono, Lavelle, and Kotzur so that the first bus means and the second bus means differ in width of address as suggested by Kato because Kato suggests that a SRAM is a high-speed memory and a DRAM is a low speed memory. Since these memories have different speeds, their buses must differ in width of address (Col. 10, lines 54-62).

26. Claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over Schlapp (US005579473A) in view of Laksono (US006288729B1), further in view of Lavelle (US006812929B2), further in view of Kotzur (US006389480B1), further in view of Yamashita (US006313844B1).

Schlapp, Laksono, Lavelle, and Kotzur are relied upon for the teachings as discussed above relative to Claim 15. Laksono describes first and second graphics engines, as discussed in the rejection for Claim 8. Lavelle describes that the graphics engine is an overlay engine, as discussed in the rejection for Claim 9.

However, Schlapp, Laksono, Lavelle, and Kotzur do not teach that the arbiter means further comprises priority means for selecting the refresh controller means as the first winning

requestor when other devices also generate a first request during the same time period. However, Yamashita describes that the arbiter means (13, Figure 9; Col. 15, line 41-Col. 16, line 9) further comprises priority means for selecting the refresh controller means (30; Col. 16, lines 41-45) as the first winning requestor when other devices also generate a first request during the same time period (Col. 1, lines 58-62).

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to modify the devices of Schlapp, Laksono, Lavelle, and Kotzur so that the arbiter means further comprises priority means for selecting the refresh controller means as the first winning requestor when other devices also generate a first request during the same time period as suggested by Yamashita because Yamashita suggests that a refresh is essential for maintaining the storage of the image signal in the image memory (Col. 1, lines 58-62).

Claim Objections

27. Claims 7, 17, and 18 are objected to because they depend from a rejected claim.

28. The following is a statement of reasons for the indication of allowable subject matter:

The prior art taken singly or in combination do not teach or suggest a frame-buffer extension in the DRAM, the frame-buffer extension for storing pixels read by the refresh controller for larger frame buffers as recited in Claims 7, 17, and 18.

29. The closest prior art (Stortz, US005900885A) teaches a DRAM (22, Figure 2) for storing graphics data and a system memory (14) with a buffer extension (42b) for storing graphics data

read by the graphics engine when there is not enough room to store it in the DRAM (Col. 2, lines 40-49). However, Stortz does not teach a frame-buffer extension in the DRAM, the frame-buffer extension for storing pixels read by the refresh controller for larger frame buffers.

30. Another prior art (Mattison, US005335322A) teaches a system memory (32, Figure 2) for storing pixels in a frame buffer (Col. 1, lines 28-31) and an optional dedicated frame buffer (40) for storing pixels for larger frame buffer (Col. 3, lines 7-9). However, Mattison does not teach that this optional dedicated frame buffer is an extension of a DRAM.

Prior Art of Record

"Multiplexer." http://en.wikipedia.org/wiki/Multiplexer.

"Video Overlay." http://www.webopedia.com/TERM/V/video_overlay.html.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joni Hsu whose telephone number is 703-305-4418. The examiner can normally be reached on M-F 8am-5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew C. Bella can be reached on 703-308-6829. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JH

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